DRIEI
PhD Program in Electronic and Computer Engineering
University of Cagliari, Italy

Course:	Formal Verification and Synthesis for Dynamical Systems: A Temporal-Logic-Based Approach
Instructor:	Xiang Yin (yinxiang@sjtu.edu.cn)
SSD:	IINF/04 – Automatic Control
Credits / hours:	0.5 credits, 4h
Language:	English
Scheduling:	Mon Sep 9, Tue Sep 10, 9:00 to 11:00, Room B_TD (ex Aula D, pad B)
Final Exam:	An assessment is scheduled.
Registration:	Interested students should register sending an email to the instructor

Goal of the Course

Formal methods rely on mathematical models to prove the correctness of systems. Temporal logic is a key tool in this domain, providing a framework to express and reason about the temporal properties of systems. The course begins with an introduction to the formal modelling of dynamic systems through labelled transition systems, focusing on how these models capture system behaviour. Students will then explore Linear Temporal Logic (LTL), learning its syntax, semantics, and how to represent LTL through automata. The course progresses to formal control synthesis, where automata-based LTL task planning and graph-game-based reactive synthesis are covered, providing tools for designing controllers that meet temporal logic specifications. Finally, a research seminar introduces Signal Temporal Logic (STL), emphasizing its use in online monitoring and model-predictive control.

Prerequisites: Discrete-event system, automata

Intersection with other courses at the University of Cagliari: None.

Course Outline

1. Formal Model of Dynamic Systems [1 h]
Labelled transition systems. Formal properties.

2. Linear Temporal logics [1 h]
Syntax and semantics of linear temporal logic (LTL), automata-based representations of LTL.

3. Formal Control Synthesis for Linear Temporal Logic Specification [1 h]
Automata-based LTL task planning, graph-game-based reactive synthesis

4. [Research Seminar] Monitoring and Control for Signal Temporal Logic Specifications [1 h]
Signal temporal logic (STL), online monitoring of STL, model-predictive control of STL

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